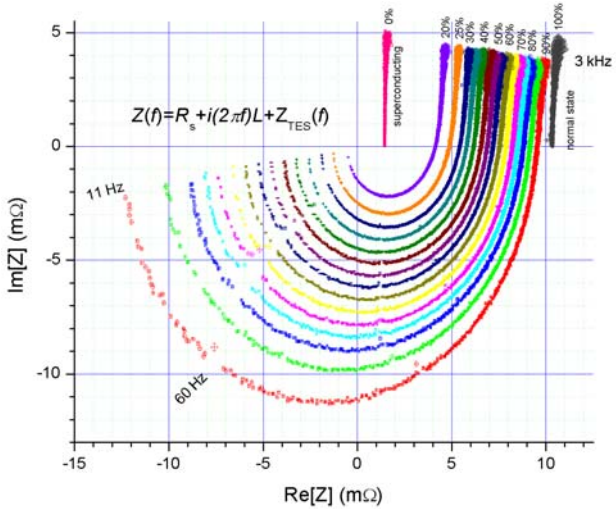
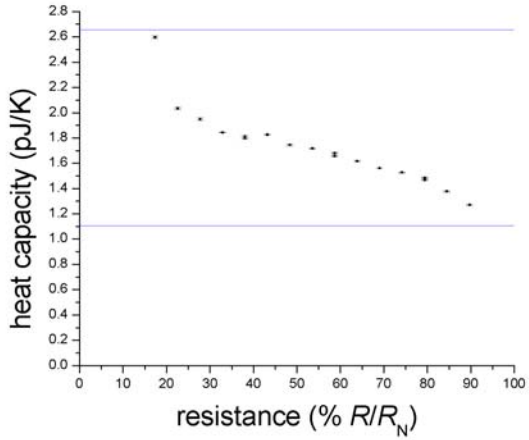
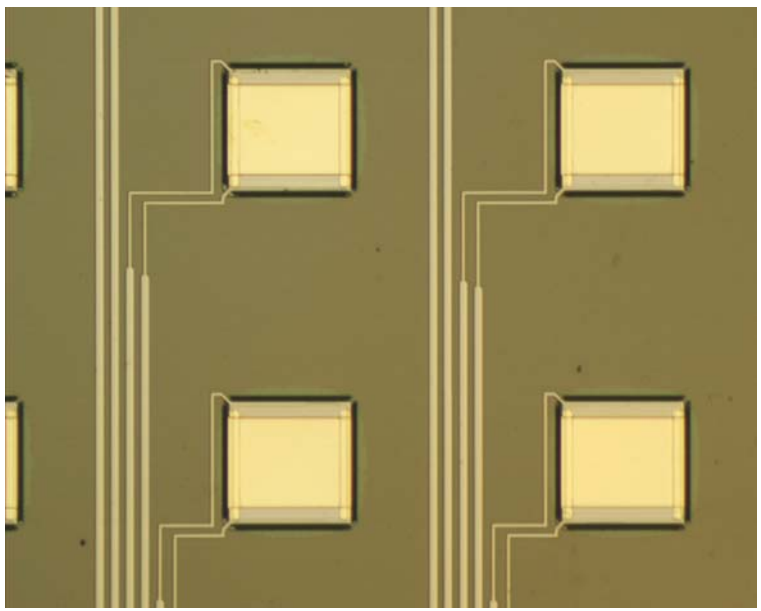
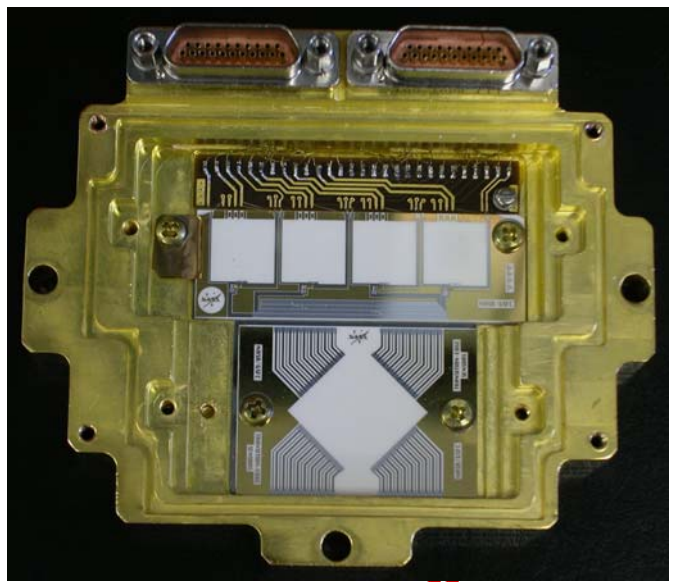
TES Microcalorimeter Development at GSFC: A Semiannual Status Report



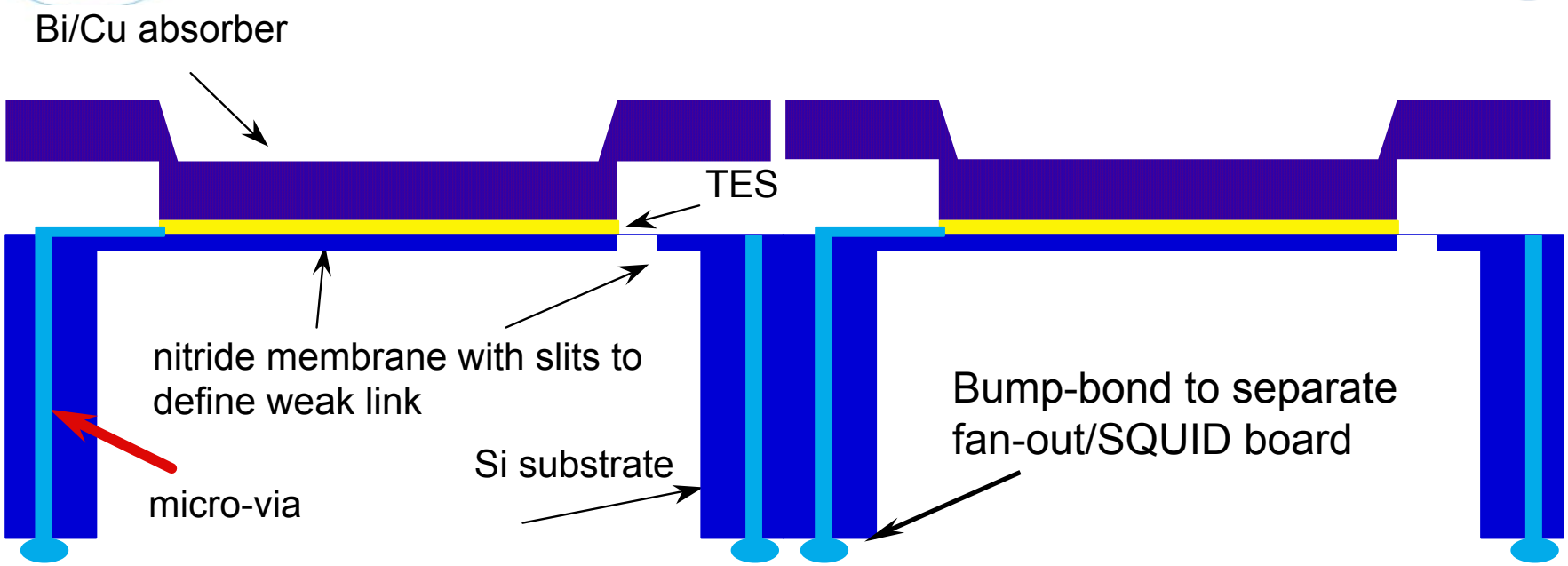


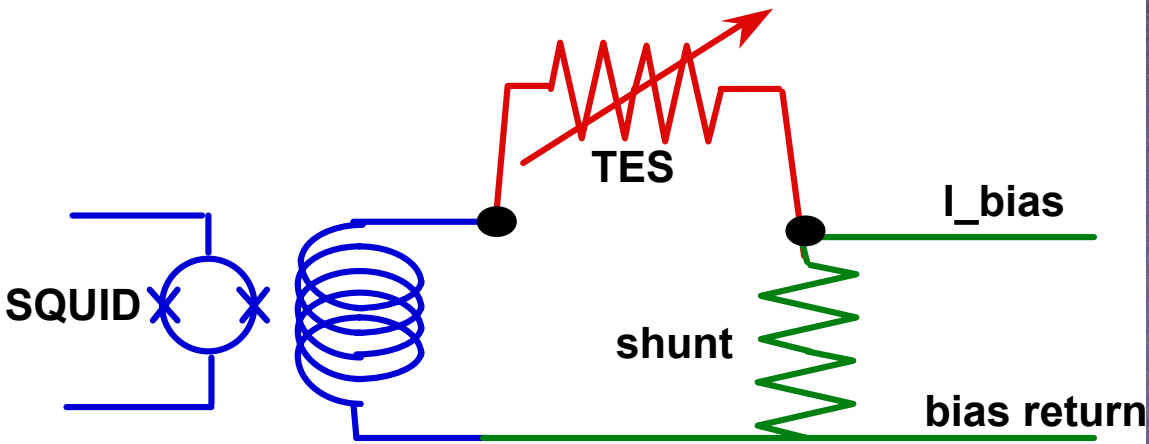


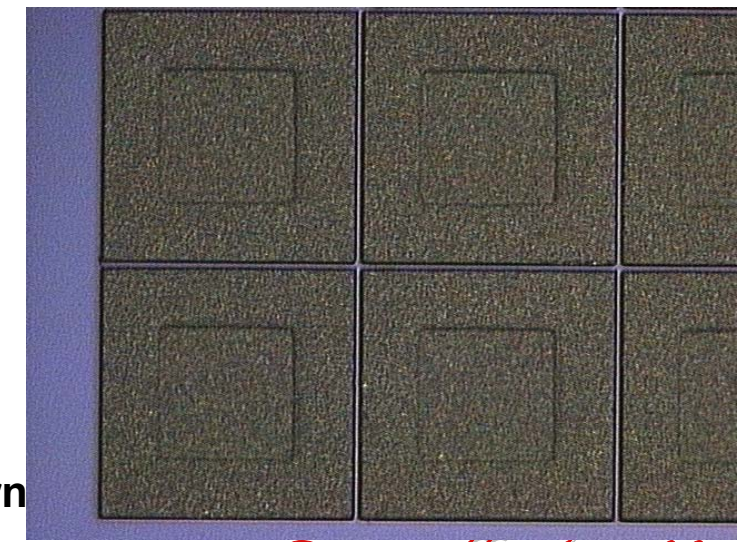
C. K. Stahle
S. Bandler
K. R. Boyce
J. A. Chervenak
E. Figueroa-Feliciano
F. M. Finkbeiner
M. Galeazzi
R. L. Kelley
M. J. Li
M. A. Lindeman
F. S. Porter
T. Stiles



Overview: TES Array Scheme







Fabrication Report

- **Tried to shift to thicker Mo/Au bilayer (50/190 nm to 65/360 nm)**
  - Motivation: put more heat capacity in the TES itself
    - Permit wider range of screening tests without absorbers
    - Simplify absorber processing
  - More "development" associated with this "simple" change than expected
    - Thicker Nb leads required for good step coverage. Can pattern using either dry-etching or lift-off
      - ~ RIE etching of thick Nb proceeded non-uniformly, thinning the nitride in the areas etched through first and yielding a confusing collection of low-G devices and shorts
      - ~ We developed a lift-off process that worked reliably with the thick Nb. It is now a robust process.
    - There appears to be a higher density of Au surface defects with the thicker Au (nodules and pinholes)
      - ~ May not be problem in itself (must investigate, noise?), but the pinholes provide a path for the Mo etch to reach the Mo under the Au, which can etch aggressively
      - ~ Pursuing both improving quality of Au and protecting the Mo underlayer with photoresist
      - ~ Will also go back to 50/190 nm for comparisons

Fabrication Report

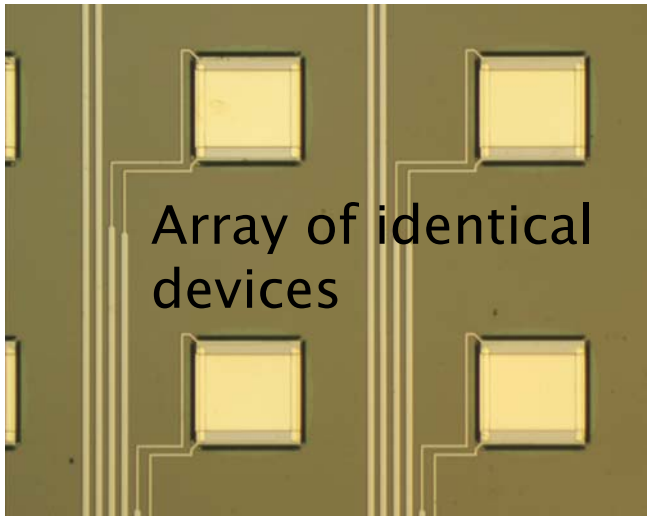
- **Unexpected short life of quartz crystal monitor (QCM)**
  - Separate QCM for the Mo and Au depositions
  - Mo QCM begins to give erroneous readings after 15% of advertised life
  - Results in thinner Mo deposition than intended, thus lower T_c
  - Simple procedural fix
  - Can get ~15 wafer depositions per QCM even with early retirement
  - We were able to bring back T_c in devices with too thin Mo by ion milling away some of the Au
- **Important lesson: CONTINUOSLY MONITOR T_C !**
  - We had ~6 wafers in process at the time the problem with the QCM reading was realized

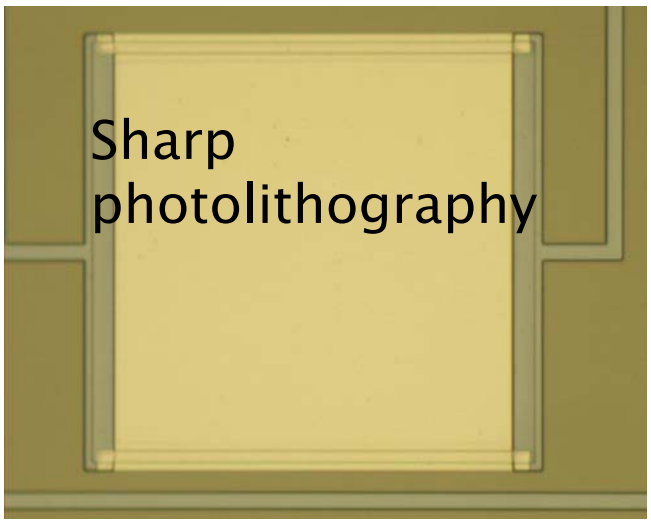
- **WE ARE CONTINUING TO LEARN ABOUT THE VARIABLES THAT AFFECT THE PROCESSING, AND WE ARE MAKING PROGRESS OPTIMIZING OUR FABRICATION PROCESS.**

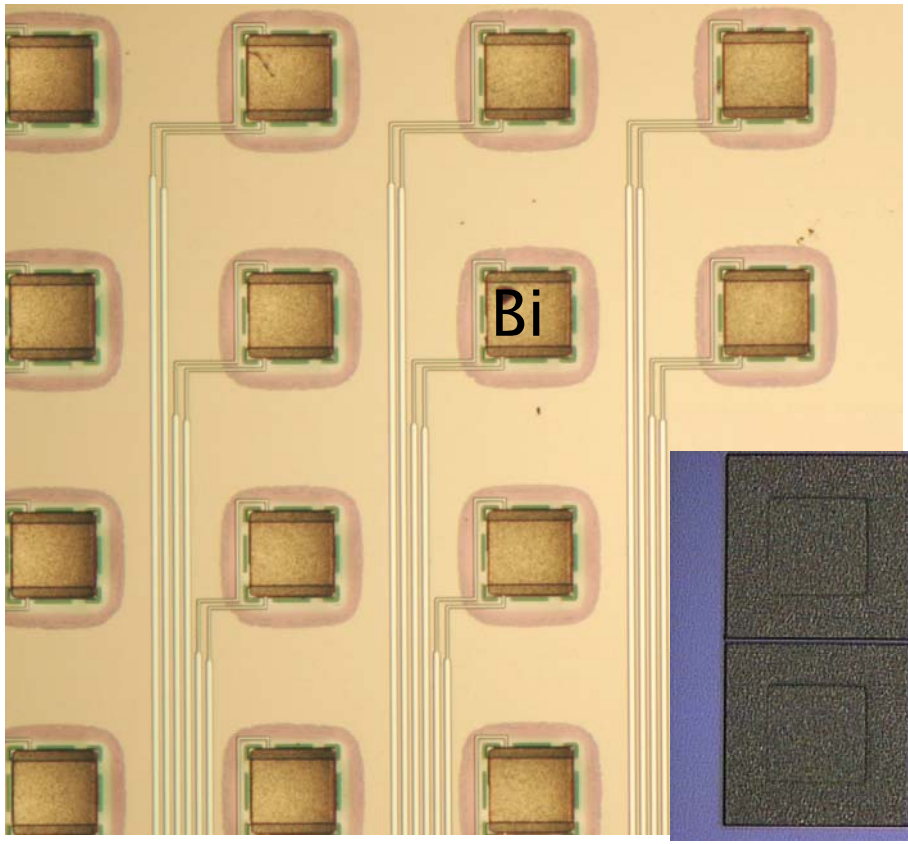
Fabrication Products in the Queue

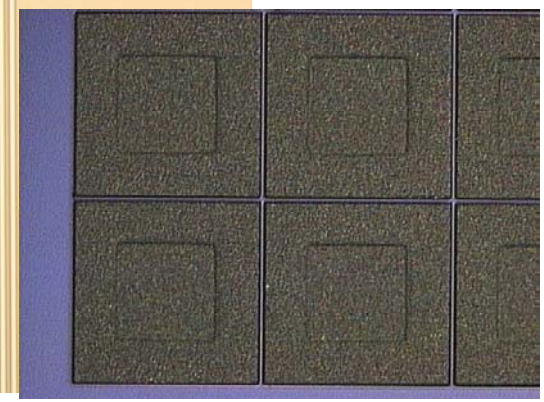
- **Compact pixels and PoSTs (same photolithography mask)**
  - GSFC immediate thrust remains that of optimizing compact pixels in a size suitable for a Constellation-X array
  - Runs for basic characterization of devices on wafers with different nitride thickness. Half of each wafer will have Bi absorbers. Dividing wafer in half along line other axis, half will have the TES boundaries defined by Au bars and half will have the boundary defined by a Mo undercut. Thus we can compare the noise of the 4 permutations, as well as get important data on thermal conductance needed to optimize the design of the compact pixels.
  - Investigations of PoSTs (imaging devices)
- **Test TES devices to investigate noise processes**
  - Different sizes and geometries
  - Schemes for engineering the phase transition
- **Test micro-vias**
  - Different sizes and geometries
  - Daisy-chains with superconducting interconnects to permit resistance measurements

Fabrication Examples



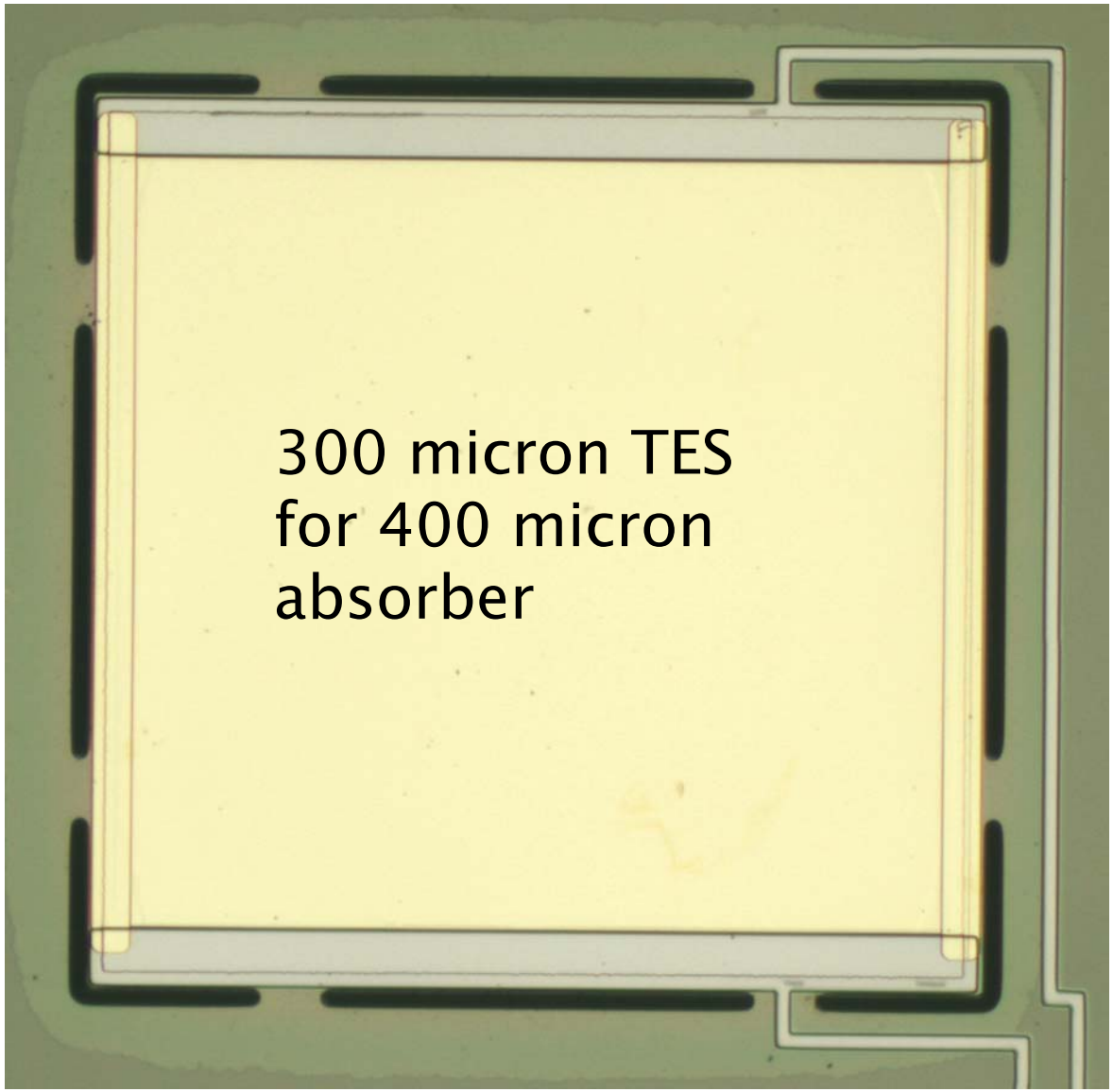


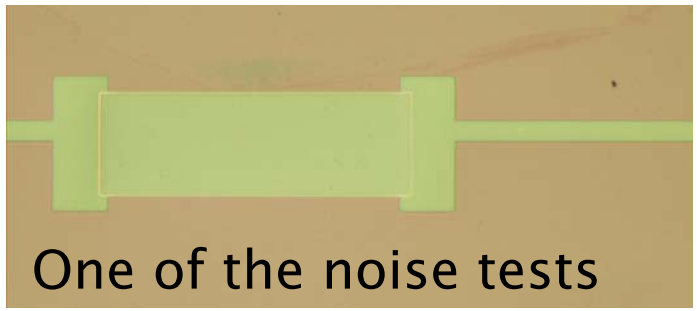




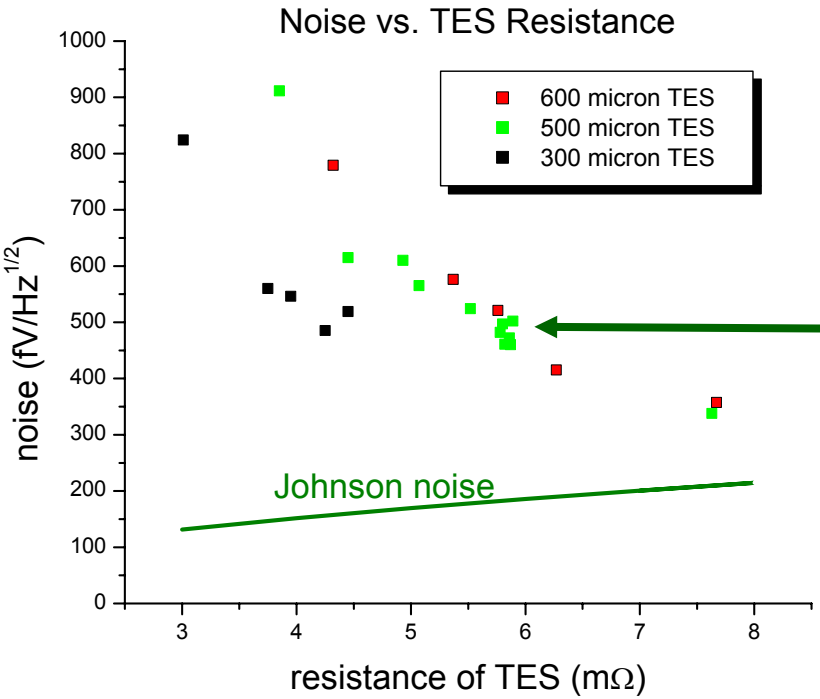
Array of identical 150 micron devices. Soon will make these with 250 and 400 micron "mushroom" absorbers. The Bi absorbers shown are the size of the stem in the mushroom.

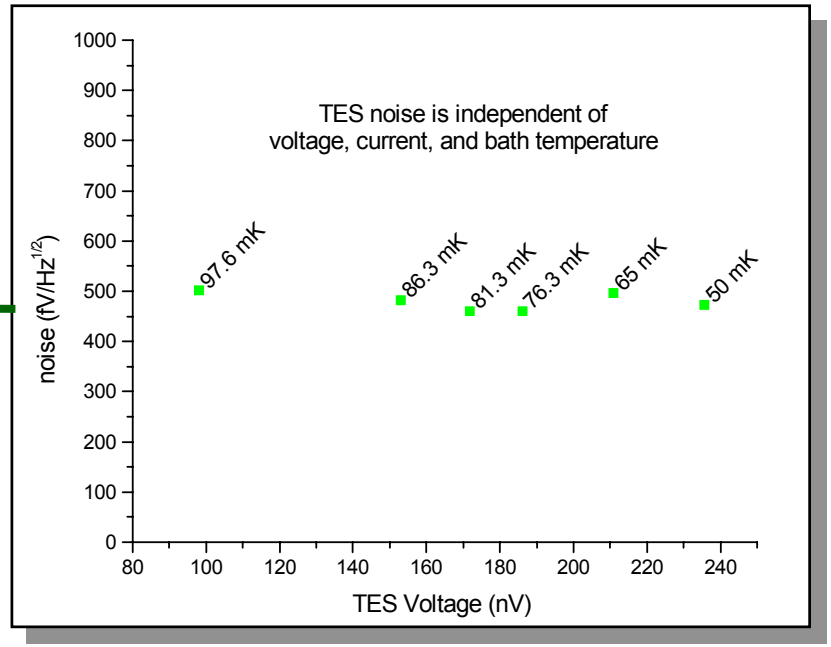
More examples



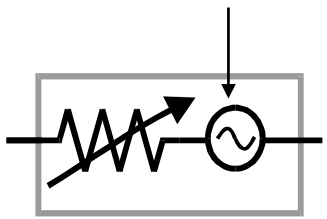


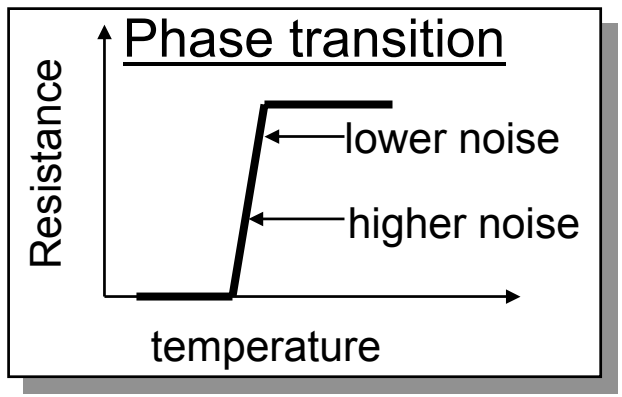
Resolution Limited By Excess Noise





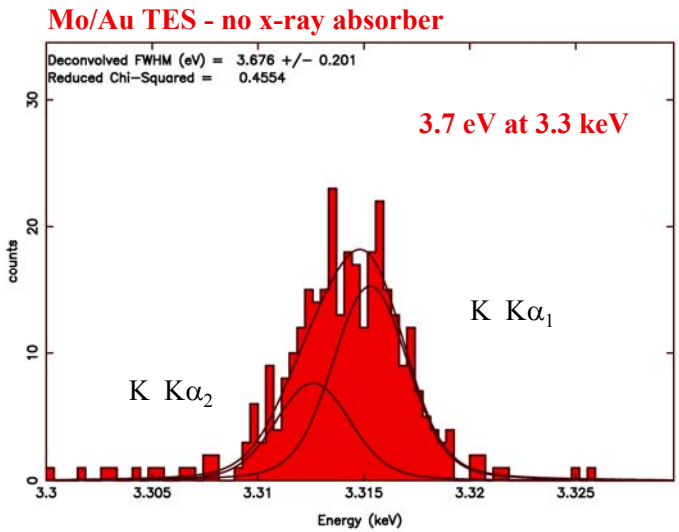
$$\text{NOISE} = n(R) \times \sqrt{4k_B TR}$$





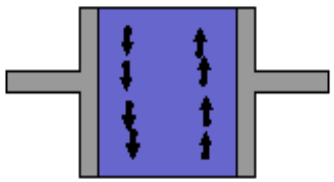
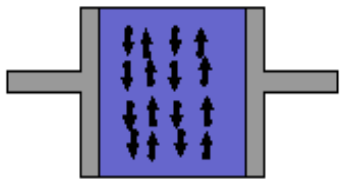
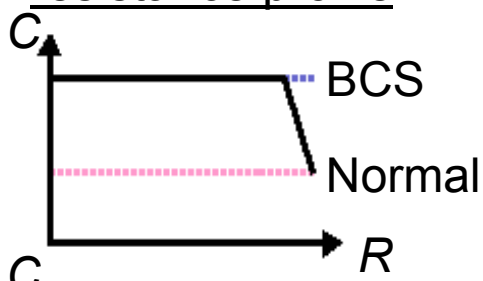
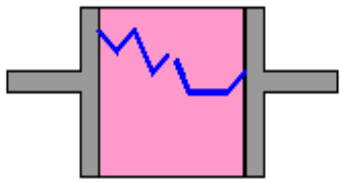
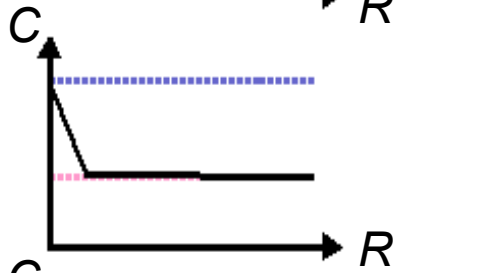
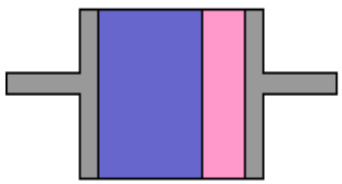
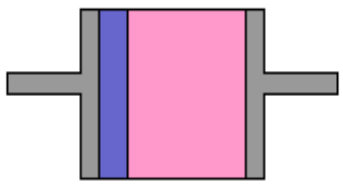
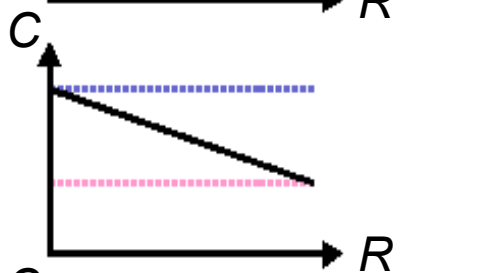
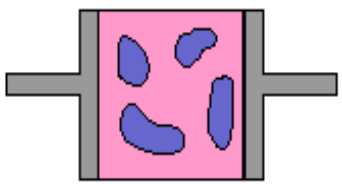
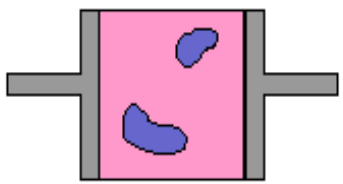
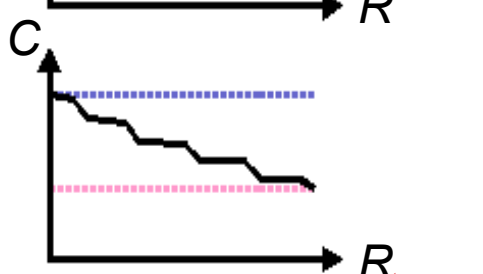
Getting at the Physics of the Noise

- **In order to eliminate the excess noise, we need to understand the physical state of the TES**
  - What is the heat capacity of a TES in the transition?
  - What is actually happening inside a TES in the phase transition?
  - What changes as the resistance changes?
  - Is it a stochastic process?
  - Can we make it more deterministic, and would that eliminate the noise?



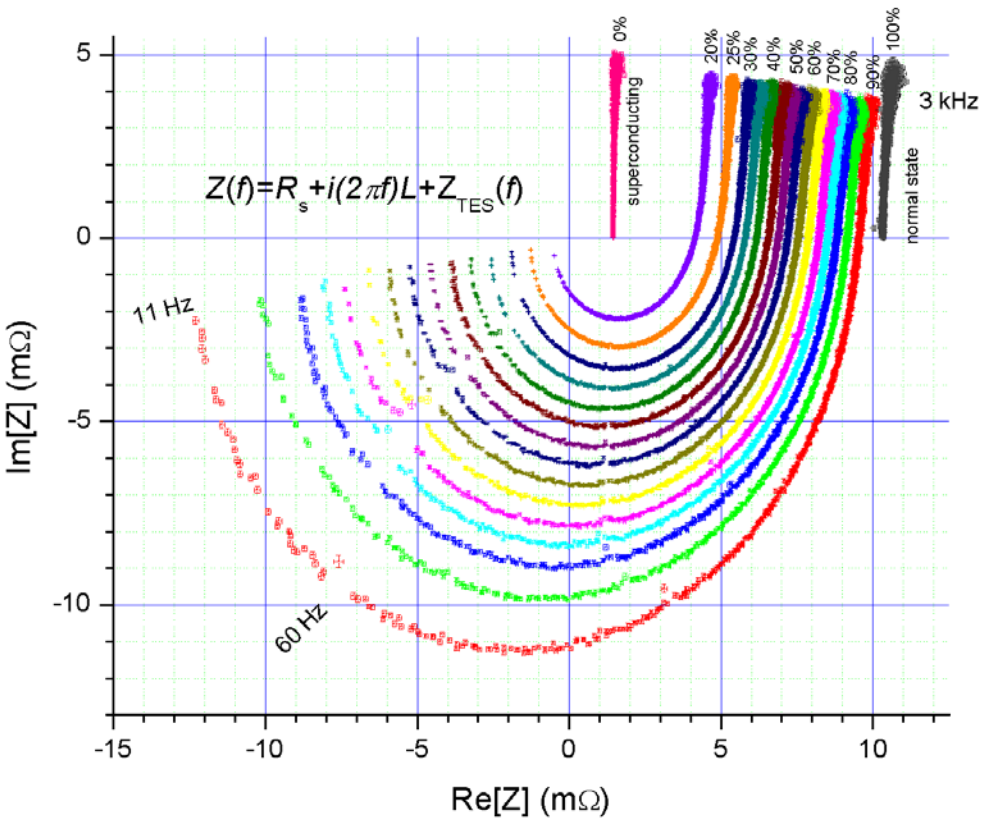
<2 eV?

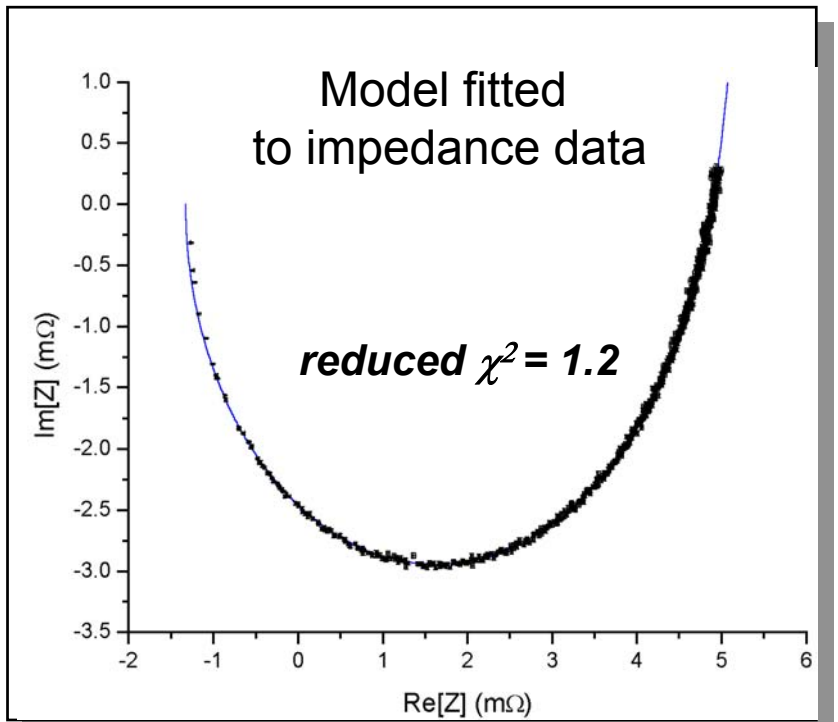
Four hypotheses about the transition

hypotheses	a possible model for each hypothesis		representative heat capacity vs. resistance profile
	Low resistance	High resistance	
Mostly superconducting with phase slips			
Mostly normal with low resistance paths			
Smooth transition part normal / part superconducting			
Chunky transition			

TES impedance measurements

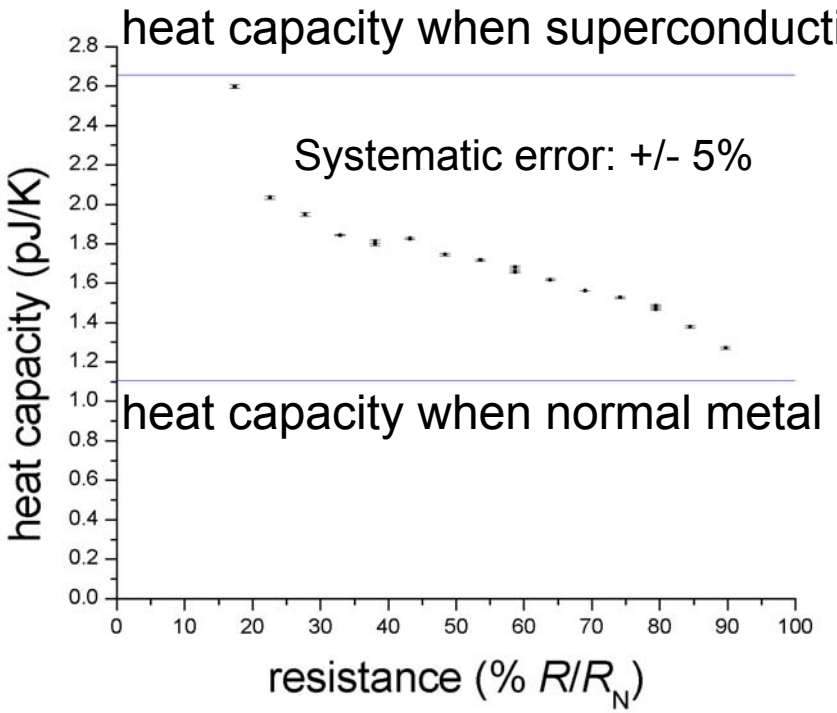
- We measure the complex impedance to characterize the TES
- Calorimeter model fits data very well
- Obtain TES heat capacity and other parameters

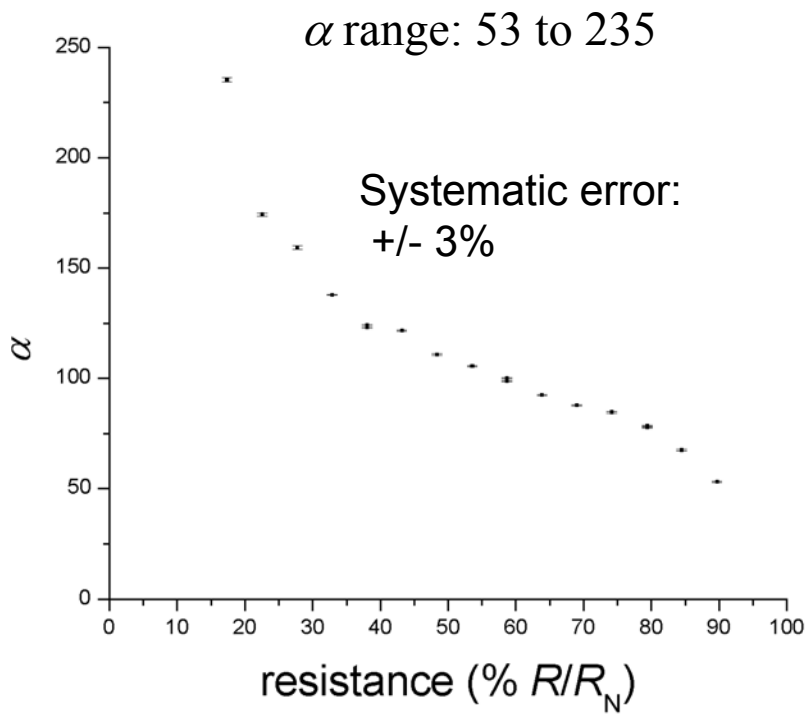




Measured calorimeter parameters

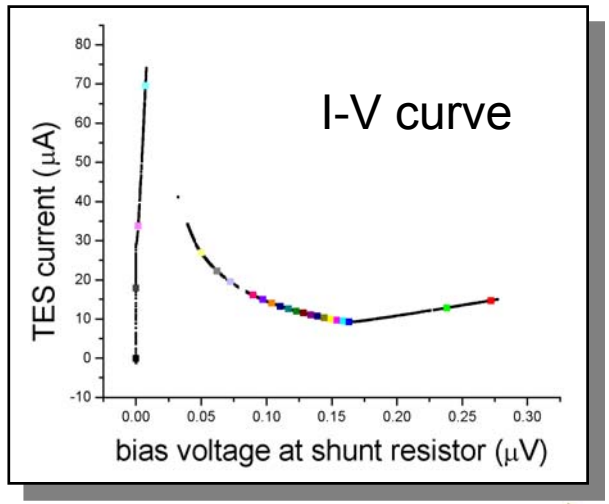
- We precisely measure heat capacity and other important parameters of TES phase transition
- Obtain information about internal state of our TESs
- Facilitates design of calorimeters for optimal performance

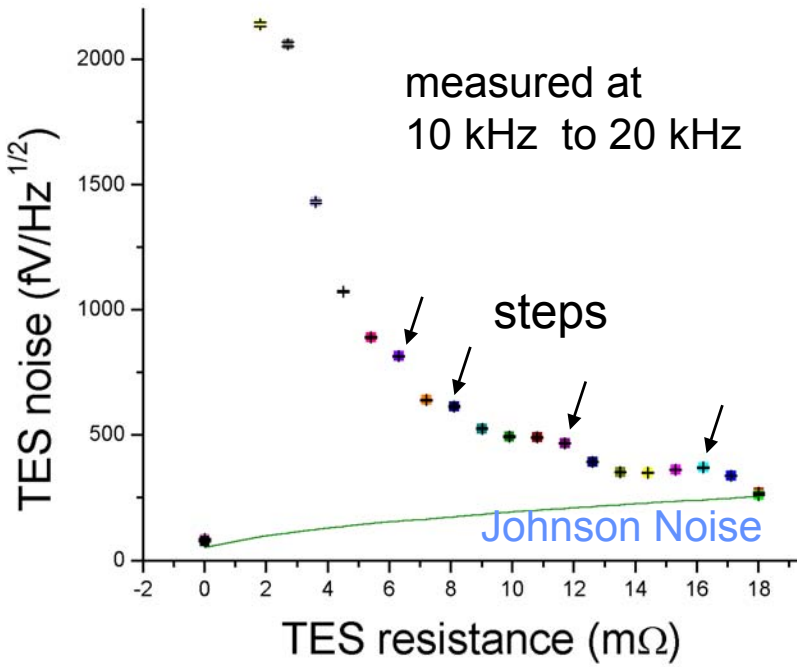


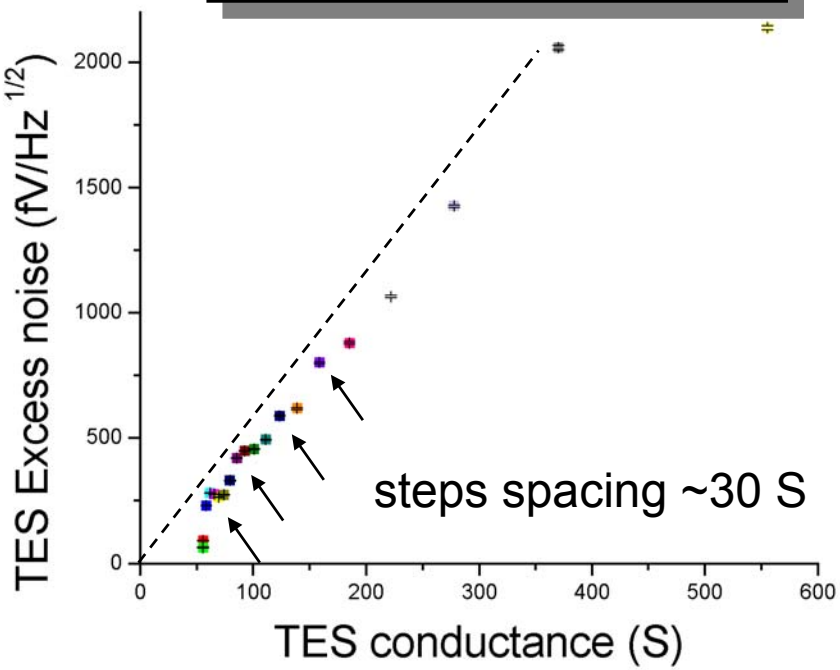


Steps in the Noise May Provide a Clue

- Excess is roughly proportional to 1/R
- Observed regular steps in noise
- I-V curve is smooth
- Observed at ~ 1kHz to 30 kHz

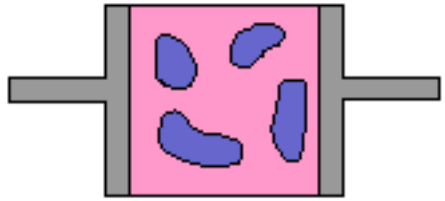


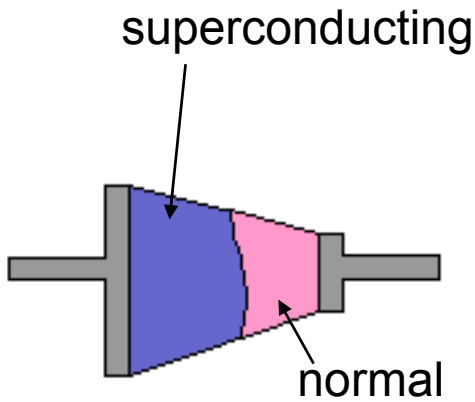




Phase separation hypothesis

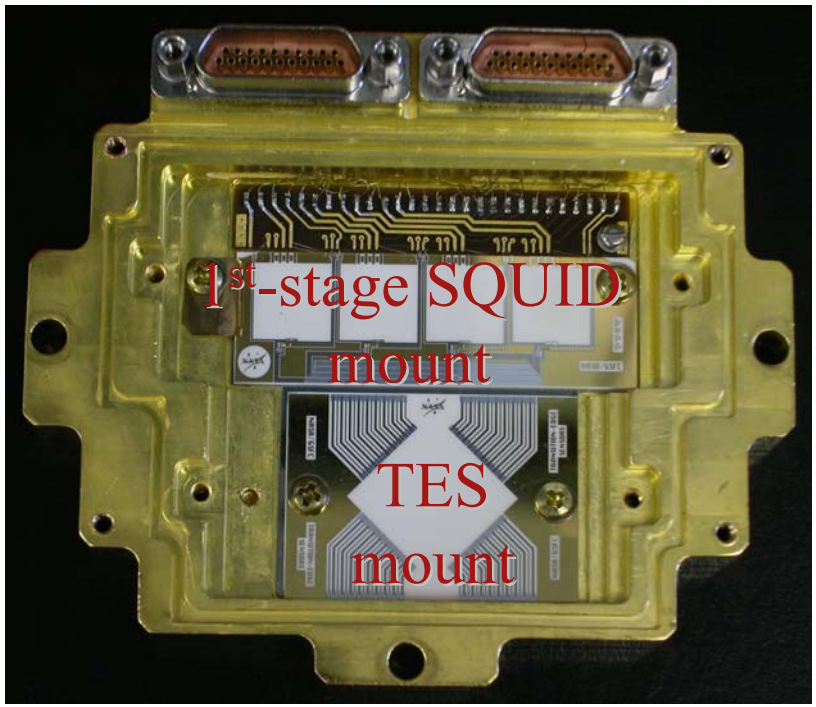
- Hypothesis: TES is separating into normal and superconducting domains
- Consistent with heat capacity measurements
- Perhaps noise steps are associated with formation of superconducting domains in the TES
- Prediction: expect to find steps in heat capacity that correlate with noise steps
- Try redesigning TES for a more orderly phase separation
- Devices on noise mask will test this prediction, as well as investigate a host of other device geometries

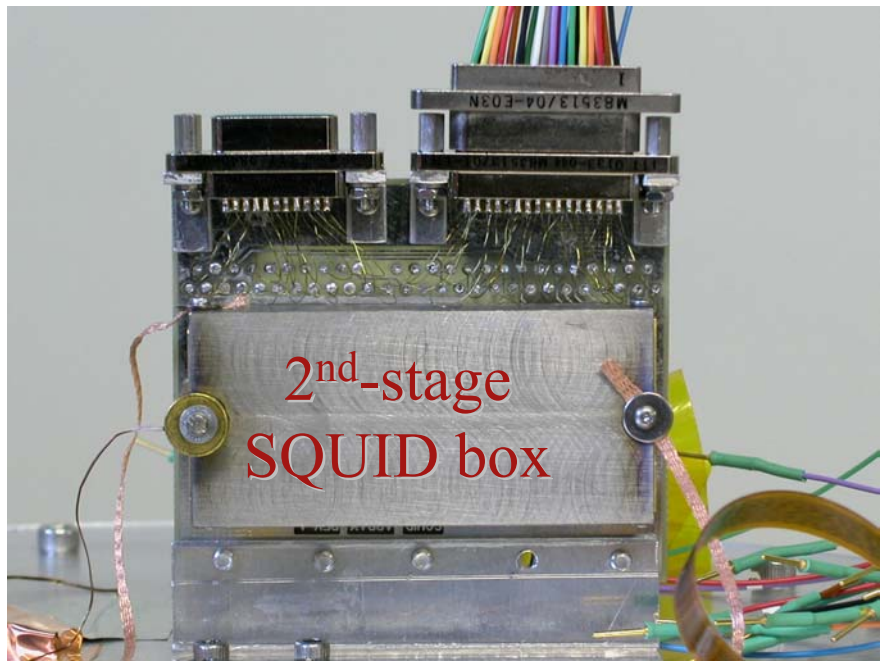




Infrastructure: Upgrading 4-channel Test Platform to 2-stage SQUID Readout

- **Needed to keep solder joints out of the TES bias circuit**
  - Superconducting wirebonds and film traces only
- **Will provide robust, reliable test platform**
- **TES mounts and first-stage SQUID mounts made in-house**
  - Alumina substrates with Au, Nb, and Al features
  - Process now worked out after initial trouble-shooting





New Infrastructure

- Beginning design of ADR platform for 2x8 demo - new member of team available to dedicate substantial time to this
- Coordinating with NIST on this demo, which will use SQUID MUX to read out a portion of an 8x8 array.
- Planning for interchangeable parts between GSFC and NIST systems so that GSFC TES arrays can be tested at NIST and vice versa
- Demo planned for end of FY '03